

## Refine Search

10/677,008

### Search Results -

Terms	Documents
(PCMO near2 layers) and ((etch or etching) near5 PCMO)	2

**Database:**

US Pre-Grant Publication Full-Text Database  
 US Patents Full-Text Database  
 US OCR Full-Text Database  
 EPO Abstracts Database  
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 IBM Technical Disclosure Bulletins

**Search:**

L4

**Refine Search**

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### Search History

**DATE:** Monday, March 21, 2005    [Printable Copy](#)    [Create Case](#)

**Set Name Query**  
side by side

**Hit Count Set Name**  
result set

*DB=USPT; PLUR=YES; OP=ADJ*

L4    (PCMO near2 layers) and ((etch or etching) near5 PCMO)  
L3    (PCMO near2 stack)  
L2    (PCMO near2 stack) and (etch or etching)  
L1    (PCMO near2 stack) and ((etch or etching) near5 PCMO)

2    L4  
 0    L3  
 0    L2  
 0    L1

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Search Results - Record(s) 1 through 2 of 2 returned.

☐ 1. Document ID: US 6774004 B1

L4: Entry 1 of 2

File: USPT

Aug 10, 2004

US-PAT-NO: 6774004

DOCUMENT-IDENTIFIER: US 6774004 B1

TITLE: Nano-scale resistance cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Draw D
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☐ 2. Document ID: US 6746910 B2

L4: Entry 2 of 2

File: USPT

Jun 8, 2004

US-PAT-NO: 6746910

DOCUMENT-IDENTIFIER: US 6746910 B2

TITLE: Method of fabricating self-aligned cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KMC	Draw D
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Clear	Generate Collection	Print	Fwd Refs	Bkwd Refs	Generate OACS
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Terms	Documents
(PCMO near2 layers) and ((etch or etching) near5 PCMO)	2

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L5: Entry 1 of 2

File: USPT

Aug 10, 2004

DOCUMENT-IDENTIFIER: US 6774004 B1

TITLE: Nano-scale resistance cross-point memory array

Detailed Description Text (12):

The first embodiment of the method of the invention uses TiN as a hard mask during etching of the memory resistor, such as PCMO. The other materials, such as SiN, TaN, WN, etc., may also be used as hard mask.

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L5: Entry 2 of 2

File: USPT

Jun 8, 2004

DOCUMENT-IDENTIFIER: US 6746910 B2

TITLE: Method of fabricating self-aligned cross-point memory array

Brief Summary Text (10):

A method of fabricating a self-aligned cross-point memory array includes preparing a substrate, including forming any supporting electronic structures; forming a swell area on the substrate; implanting ions to form a deep N.sup.+ region; implanting ions to form a shallow P+ region on the N.sup.+ region to form a P+/N junction; depositing a barrier metal layer on the P+ region; depositing a bottom electrode layer on the barrier metal layer; depositing a sacrificial layer of polysilicon or silicon nitride on the bottom electrode layer; patterning and etching the structure to remove portions of the polysilicon layer, the bottom electrode layer, the barrier metal layer, the P+ region and the N.sup.+ region to form a trench; depositing oxide to fill the trench; patterning and etching the polysilicon; depositing a PCMO layer which is self-aligned with the remaining bottom electrode layer; depositing a top electrode layer; patterning and etching the top electrode layer; and completing the memory array structure.

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☐ 1. Document ID: US 6774004 B1

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File: USPT

Aug 10, 2004

US-PAT-NO: 6774004

DOCUMENT-IDENTIFIER: US 6774004 B1

TITLE: Nano-scale resistance cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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☐ 2. Document ID: US 6746910 B2

L5: Entry 2 of 2

File: USPT

Jun 8, 2004

US-PAT-NO: 6746910

DOCUMENT-IDENTIFIER: US 6746910 B2

TITLE: Method of fabricating self-aligned cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KWIC	Draw D
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Terms	Documents
PCMO near3 (etching or etch)	2

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**Hit Count Set Name**

result set

*DB=USPT; PLUR=YES; OP=ADJ*

<u>L5</u>	PCMO near3 (etching or etch)	2	<u>L5</u>
<u>L4</u>	(PCMO near2 layers) and ((etch or etching) near5 PCMO)	2	<u>L4</u>
<u>L3</u>	(PCMO near2 stack)	0	<u>L3</u>
<u>L2</u>	(PCMO near2 stack) and (etch or etching)	0	<u>L2</u>
<u>L1</u>	(PCMO near2 stack) and ((etch or etching) near5 PCMO)	0	<u>L1</u>

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L7: Entry 1 of 1

File: USPT

Feb 17, 2004

DOCUMENT-IDENTIFIER: US 6693821 B2

TITLE: Low cross-talk electrically programmable resistance cross point memory

## CLAIMS:

7. A memory structure comprising; a) a silicon substrate; b) a plurality of platinum bottom electrodes overlying the substrate; c) a plurality of platinum top electrodes overlying the bottom electrodes, wherein the top electrodes cross over the bottom electrodes forming a cross point at each cross over location; and d) a single layer of Pr.sub.0.7 Ca.sub.0.3 MnO.sub.3 (PCMO) interposed between the plurality of top electrodes and the plurality of bottom electrodes at each cross point.

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## Refine Search

### Search Results -

Terms	Documents
(top near2 electrode) and (bottom near2 electrode) and PCMO and (etch or etching)	12

Database:

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Search:

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### Search History

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<u>Set</u> <u>Name</u> side by side	<u>Query</u>	<u>Hit</u> <u>Count</u>	<u>Set</u> <u>Name</u> result set
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
<u>L9</u>	(top near2 electrode) and (bottom near2 electrode) and PCMO and (etch or etching)	12	<u>L9</u>
<u>L8</u>	17 and etch	0	<u>L8</u>
<u>L7</u>	(plurality near4 PCMO)	1	<u>L7</u>
<u>L6</u>	(stacks or stack) near9 PCMO	0	<u>L6</u>
<u>L5</u>	PCMO near3 (etching or etch)	2	<u>L5</u>
<u>L4</u>	(PCMO near2 layers) and ((etch or etching) near5 PCMO)	2	<u>L4</u>
<u>L3</u>	(PCMO near2 stack)	0	<u>L3</u>
<u>L2</u>	(PCMO near2 stack) and (etch or etching)	0	<u>L2</u>
<u>L1</u>	(PCMO near2 stack) and ((etch or etching) near5 PCMO)	0	<u>L1</u>

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☐ 1. Document ID: US 6859382 B2

L9: Entry 1 of 12

File: USPT

Feb 22, 2005

US-PAT-NO: 6859382

DOCUMENT-IDENTIFIER: US 6859382 B2

TITLE: Memory array of a non-volatile ram

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWD	Draw D
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☐ 2. Document ID: US 6858905 B2

L9: Entry 2 of 12

File: USPT

Feb 22, 2005

US-PAT-NO: 6858905

DOCUMENT-IDENTIFIER: US 6858905 B2

TITLE: Methods of manufacturing low cross-talk electrically programmable resistance cross point memory structures

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWD	Draw D
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☐ 3. Document ID: US 6856536 B2

L9: Entry 3 of 12

File: USPT

Feb 15, 2005

US-PAT-NO: 6856536

DOCUMENT-IDENTIFIER: US 6856536 B2

TITLE: Non-volatile memory with a single transistor and resistive memory element

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	KWD	Draw D
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☐ 4. Document ID: US 6841833 B2

L9: Entry 4 of 12

File: USPT

Jan 11, 2005

US-PAT-NO: 6841833

DOCUMENT-IDENTIFIER: US 6841833 B2

TITLE: 1T1R resistive memory

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 5. Document ID: US 6825058 B2

L9: Entry 5 of 12

File: USPT

Nov 30, 2004

US-PAT-NO: 6825058

DOCUMENT-IDENTIFIER: US 6825058 B2

TITLE: Methods of fabricating trench isolated cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 6. Document ID: US 6809753 B2

L9: Entry 6 of 12

File: USPT

Oct 26, 2004

US-PAT-NO: 6809753

DOCUMENT-IDENTIFIER: US 6809753 B2

TITLE: Optical microswitch printer heads

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 7. Document ID: US 6774054 B1

L9: Entry 7 of 12

File: USPT

Aug 10, 2004

US-PAT-NO: 6774054

DOCUMENT-IDENTIFIER: US 6774054 B1

TITLE: High temperature annealing of spin coated Pr1-xCaxMnO3 thim film for RRAM application

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 8. Document ID: US 6774004 B1

L9: Entry 8 of 12

File: USPT

Aug 10, 2004

US-PAT-NO: 6774004

DOCUMENT-IDENTIFIER: US 6774004 B1

TITLE: Nano-scale resistance cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 9. Document ID: US 6762481 B2

L9: Entry 9 of 12

File: USPT

Jul 13, 2004

US-PAT-NO: 6762481

DOCUMENT-IDENTIFIER: US 6762481 B2

TITLE: Electrically programmable nonvolatile variable capacitor

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	DOC	Draw D
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☐ 10. Document ID: US 6746910 B2

L9: Entry 10 of 12

File: USPT

Jun 8, 2004

US-PAT-NO: 6746910

DOCUMENT-IDENTIFIER: US 6746910 B2

TITLE: Method of fabricating self-aligned cross-point memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference	Claims	DOC	Draw D
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Terms	Documents
(top near2 electrode) and (bottom near2 electrode) and PCMO and (etch or etching)	12

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☐ 11. Document ID: US 6583003 B1

L9: Entry 11 of 12

File: USPT

Jun 24, 2003

US-PAT-NO: 6583003

DOCUMENT-IDENTIFIER: US 6583003 B1

TITLE: Method of fabricating 1T1R resistive memory array

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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☐ 12. Document ID: US 6204139 B1

L9: Entry 12 of 12

File: USPT

Mar 20, 2001

US-PAT-NO: 6204139

DOCUMENT-IDENTIFIER: US 6204139 B1

TITLE: Method for switching the properties of perovskite materials used in thin film resistors

Full	Title	Citation	Front	Review	Classification	Date	Reference			Claims	KMC	Draw D
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Terms	Documents
(top near2 electrode) and (bottom near2 electrode) and PCMO and (etch or etching)	12

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